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Attorney Docket No. 00791/LH

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): T. WAKABAYASHI

Serial No. : 09/704,156

Filed : November 1, 2000

For : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Art Unit : 2827

Examiner : Luan C. Thai

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date noted below.

S. Dianne Franklin

Dated: April 26, 2002

In the event that this Paper is late filed, and the necessary petition for extension of time is not filed concurrently herewith, please consider this as a Petition for the requisite extension of time, and to the extent not tendered by check attached hereto, authorization to charge the extension fee, or any other fee required in connection with this Paper, to Account No. 06-1378.

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R :

This is responsive to the Office Action mailed February 7, 2002, the term for response to which expires on May 7, 2002.

IN THE CLAIMS

Please cancel claims 1-~~17~~ 16, without prejudice; and please add new claims 17-37 as follows:

A1

17. (New) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip-forming regions, a lower surface opposing the

upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench extending at least half a thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a first seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled and such that a top surface of each of the outer connection terminals is exposed;

forming a second seal film on the lower surface of the semiconductor wafer; and

cutting the first seal film along the trenches by removing parts of the first seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the first seal film provided on an upper surface thereof and at least on an upper part of a periphery thereof, and each of which has the second seal film provided on the lower surface thereof.

18. (New) The method according to claim 17, further comprising:

adhering a dicing tape to the semiconductor wafer before the trenches are made in the semiconductor wafer.

19. (New) The method according to claim 18, further comprising:

adhering a support tape to an upper surface of the first seal film after the first seal film is cut; and

peeling the dicing tape from the semiconductor wafer.

20. (New) The method according to claim 17, further comprising:

polishing the lower surface of the semiconductor wafer before the second seal film is formed on the lower surface of the semiconductor wafer, thereby reducing a thickness of the semiconductor wafer.

A1 Cont.

21. (New) The method according to claim 18, wherein the trenches are formed so as to cut the semiconductor wafer completely in a thickness direction and to form concavities in an upper portion of the dicing tape.

22. (New) The method according to claim 21, wherein the first seal film is formed so as to fill in the concavities in the upper portion of the dicing film.

23. (New) The method according to claim 22, further comprising:

peeling off the dicing tape from the semiconductor film; and

removing the first seal film from the concavities in the upper portion of the dicing film.

24. (New) The method according to claim 17, further comprising:

polishing the lower surface of the semiconductor wafer to reach up to the trenches.

25. (New) The method according to claim 17, wherein the first seal film is first formed on the upper surface of the semiconductor wafer so as to cover the top surface of each of the outer connection terminals, and wherein an upper surface of the first seal film is then polished until the top surface of each of the outer connection terminals is exposed.

A1 Cont.

26. (New) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of connection pads formed on the upper surface;

forming on the upper surface of the semiconductor wafer an insulating film having openings such that the upper surface of the semiconductor wafer is covered and the connection pads are exposed via the openings;

forming on the insulating film wirings connected to the connection pads;

forming pillar-shaped electrodes on the wirings;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench extending at least half a thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled and such that a top surface of each of the pillar-shaped electrodes is exposed; and

A1 Com.

cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the seal film provided on an upper surface thereof and at least on an upper part of a periphery thereof while leaving a lower part of the periphery thereof exposed.

27. (New) The method according to claim 26, further comprising:

forming another seal film on the lower surface of the semiconductor wafer, before cutting the seal film along the trenches.

28. (New) The method according to claim 26, wherein the seal film is first formed on the upper surface of the semiconductor wafer so as to cover the top surface of each of the pillar-shaped electrodes, and wherein an upper surface of the seal film is then polished until the top surface of each of the pillar-shaped electrodes is exposed.

A1 cont.

29. (New) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, a thickness between the upper and lower surfaces, and a plurality of pillar-shaped electrodes formed on the upper surface;

adhering a dicing tape to the lower surface of the semiconductor wafer;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending to the dicing tape in part through the thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a seal film on the upper surface of the semiconductor wafer so as to fill in the trenches and cover the pillar-shaped electrodes;

polishing an upper surface of the seal film until a top surface of each of the pillar-shaped electrodes is exposed; and

cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches.

30. (New) The method according to claim 29, wherein cutting of the seal film is terminated at a position such that a full thickness of the dicing tape is not cut.

A1 cont.

31. (New) The method according to claim 30, further comprising:

adhering a support tape to the upper surface of the seal film after cutting the seal film along the trenches.

32. (New) The method according to claim 31, further comprising:

peeling off the dicing tape from the lower surface of the semiconductor wafer after adhering the support tape to the upper surface of the seal film.

33. (New) The method according to claim 32, further comprising:

polishing the lower surface of the semiconductor wafer after peeling off the dicing tape.

34. (New) The method according to claim 33, further comprising:

obtaining individual semiconductor devices separated from one another by peeling off the support tape.

35. (New) A method of manufacturing a semiconductor device comprising:

A1 cont.

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, a thickness between the upper and lower surfaces, and a plurality of pillar-shaped electrodes formed on the upper surface;

forming a rear seal film on the lower surface of the semiconductor wafer;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending to the rear seal film in part through the thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a front seal film on the upper surface of the semiconductor wafer so as cover the upper surface of the semiconductor wafer while leaving a top surface of each of the pillar-shaped electrodes exposed, and so as to fill in the

trenches and thereby entirely enclose each of the chip-forming regions within the front seal film and the rear seal film; and

cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches.

36. (New) The method according to claim 35, further comprising:

adhering a tape to the rear seal film before making the trenches.

37. (New) The method according to claim 35, wherein the front seal film is first formed on the upper surface of the semiconductor wafer so as to cover the top surface of each of the pillar-shaped electrodes, and wherein an upper surface of the first seal film is then polished until the top surface of each of the pillar-shaped electrodes is exposed.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

THE CLAIMS

Claims 1-16 have been canceled, without prejudice, and new claims 17-37 have been added to more clearly recite the patentably distinguishing features of the present invention in better U.S. form.

It is respectfully submitted that no new matter has been added, and it is respectfully requested that the new claims be approved and entered.

The patentably distinguishing features of each of new independent claims 17, 26, 29 and 35 are described in detail hereinbelow.

Claim 17

New independent claim 17 has been prepared to clarify that the method of manufacturing a semiconductor device according to one embodiment of the present invention comprises forming a first seal film on the upper surface of a semiconductor wafer, forming a second seal film on the lower surface of the semiconductor wafer, and cutting the first seal film along trenches by removing parts of the first seal film having a smaller width than the trenches such that the semiconductor wafer is separated into

individual semiconductor devices, each of which has the first seal film provided on an upper surface thereof and at least on an upper part of a periphery thereof, and each of which has the second seal film provided on the lower surface thereof.

With this method, semiconductor devices can be prepared with their upper, lower and side surfaces all covered by the seal films, only by cutting the semiconductor wafer along the trenches. Thus, in contrast to the conventional method of forming a seal film on the back of each semiconductor device after dicing, the method of the present invention as recited in new independent claim 17 can greatly improve productivity.

And it is respectfully submitted that the present invention as recited in new independent claim 17 patentably distinguishes over USP 5,989,982 ("Yoshikazu") and USP 5,888,883 ("Sasaki et al") which were cited by the Examiner against original (now canceled) claims 11-15.

With respect to Yoshikazu, it is noted that this reference does not at all disclose, teach or suggest forming a seal film on the back surface of a semiconductor wafer, as according to the present invention as recited in new independent claim 17. As illustrated in Fig. 1 of Yoshikazu, each semiconductor device obtained after dicing a wafer has a seal film only on its top and side surfaces. Thus, since no seal film is deposited on the back in this structure, it is necessary to place the film on each

device individually when back side sealing needs to be performed. This results in low productivity.

And with respect to Sasaki et al, it is noted that this reference was only cited by the Examiner against original (now canceled) claims 13 and 14 for the disclosure of adhering a support tape to an upper surface of a seal film after the seal film is cut, and then polishing the lower surface of the semiconductor wafer. This reference, however, does not at all disclose, teach or suggest forming a seal film on the back surface of a semiconductor wafer, as according to the present invention as recited in new independent claim 17.

Accordingly, it is respectfully submitted that the present invention as recited in new independent claim 17, as well as each of new claims 18-25 depending therefrom, patentably distinguishes over Yoshikazu and Sasaki et al, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

Claim 26

New independent claim 26 has been prepared to clarify that the method of manufacturing a semiconductor device according to another embodiment of the present invention comprises making trenches which extend at least half a thickness of a semiconductor wafer, forming a seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled and such that the top surfaces of pillar-shaped electrodes are

exposed, and cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the seal film provided on an upper surface thereof and at least on an upper part of a periphery thereof while leaving a lower part of the periphery thereof exposed.

In this connection, it is noted that when forming trenches in a semiconductor wafer, it is difficult to insert a blade precisely down to the boundary between the wafer and the dicing tape. The method of this type requires fine tolerances in use of a dicing machine with respect to a semiconductor wafer. If the blade needs to be stopped exactly at the boundary, productivity is significantly lowered.

Thus, according to the method of the present invention as recited in new independent claim 26, the trenches are completed by cutting the wafer either in part or to half the thickness of the wafer. This means that, in the process of cutting the wafer into separate devices, the wafer thickness becomes the maximum tolerance. As a result, the method of the present invention as recited in new independent claim 26 can greatly improve productivity.

And it is respectfully submitted that the present invention as recited in new independent claim 26 patentably distinguishes

over USP 6,159,837 ("Yamaji et al") and Yoshikazu which were cited by the Examiner against original (now canceled) claim 16.

With respect to Yamaji, it is noted that none of the embodiments disclosed in Figs. 1A-2C, 2A, 2B, and 3-6 thereof incorporates a seal film on the side surfaces of the semiconductor device 1.

And with respect to Yoshikazu, it is noted that the seal film 3 covers the entire side surfaces (from the top through the bottom) of the semiconductor device 1, as illustrated in Fig. 1 thereof.

Accordingly, it is respectfully submitted that neither Yamaji et al nor Yoshikazu discloses, teaches or suggests the above described features of the present invention as recited in new independent claim 26, and that new independent claim 26 and each of new claims 27 and 28 depending therefrom patentably distinguish over Yamaji et al and Yoshikazu, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

Claim 29

New independent claim 29 has been prepared to clarify that the method of manufacturing a semiconductor device according to another embodiment of the present invention comprises making trenches which successively extend to a dicing tape in part through a thickness of a semiconductor wafer, forming a seal film on the upper surface of the semiconductor wafer so as to fill in

the trenches and cover pillar-shaped electrodes, polishing an upper surface of the seal film until a top surface of each of the pillar-shaped electrodes is exposed, and cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches.

In this connection, it is again noted that it is difficult to stop a blade at the boundary between a dicing tape and a semiconductor wafer to cut trenches into the wafer. For this reason, according to the method of the present invention as recited in new independent claim 29, the trenches are prepared so as to extend to the dicing tape in part through the thickness of the wafer, and when the wafer is diced the thickness of the wafer is the maximum tolerance. This greatly improves productivity.

As can be seen in Fig. 1 of Yoshikazu, the seal film 3 thereof formed on the sides of the semiconductor device 1 does not have a portion extending from the bottom surface of the device. This means that this reference does not disclose, teach or suggest forming trenches in the manner of the present invention as recited in new independent claim 29.

In addition, it is pointed out that neither Yoshikazu nor Yamaji et al discloses, teaches or suggests, polishing an upper surface of a seal film until top surfaces of pillar-shaped electrodes are exposed, as according to the present invention as recited in new independent claim 29.

Accordingly, it is respectfully submitted that the present invention as recited in new independent claim 29 and each of new

claims 30-34 depending therefrom patentably distinguishes over Yamaji et al and Yoshikazu, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

Claim 35

New independent claim 35 has been prepared to clarify that the method of manufacturing a semiconductor device according to another embodiment of the present invention comprises forming a rear seal film on the lower surface of a semiconductor wafer, making trenches which successively extending to the rear seal film in part through a thickness of the semiconductor wafer, and forming a front seal film on the upper surface of the semiconductor wafer so as cover the upper surface of the semiconductor wafer while leaving a top surface of each of the pillar-shaped electrodes exposed, and so as to fill in the trenches and thereby entirely enclose each of the chip-forming regions within the front seal film and the rear seal film.

It is respectfully submitted that neither Yoshikazu nor Yamaji et al discloses, teaches or suggests the above described features of the present invention as recited in new independent claim 35, and that new independent claim35 and each of new claims 36 and 37 depending therefrom patentably distinguish over Yamaji et al and Yoshikazu, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

CLAIM FEE

The application was originally filed with 16 claims of which 4 were independent, and the appropriate claim fee was paid for such claims. The application now contains 21 claims, of which 4 are again independent. Accordingly, a claim fee in the amount of $18.00 for the addition of 1 extra claim in total is attached hereto. In addition, authorization is hereby given to charge any additional fees which may be determined to be required to Account No. 06-1378.

Re: PRIORITY CLAIM

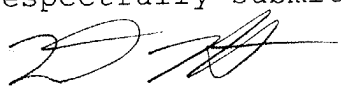
It is respectfully requested that the Examiner acknowledge receipt of the certified priority document which was filed in the Patent Office on November 1, 2000, concurrently with the filing of the original application papers.

* *

In view of the foregoing, entry of the Amendment, allowance of the claims, and the passing of the application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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